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| KSU_logo.jpg | **King Saud University**  **College of Computer and Information Sciences**  **Department of Computer Science** |

**CSC 220: Computer Organization**

**Labwork - #6**

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1. **Introduction**

In this lab we see the plexers and we design some of the famous circuits

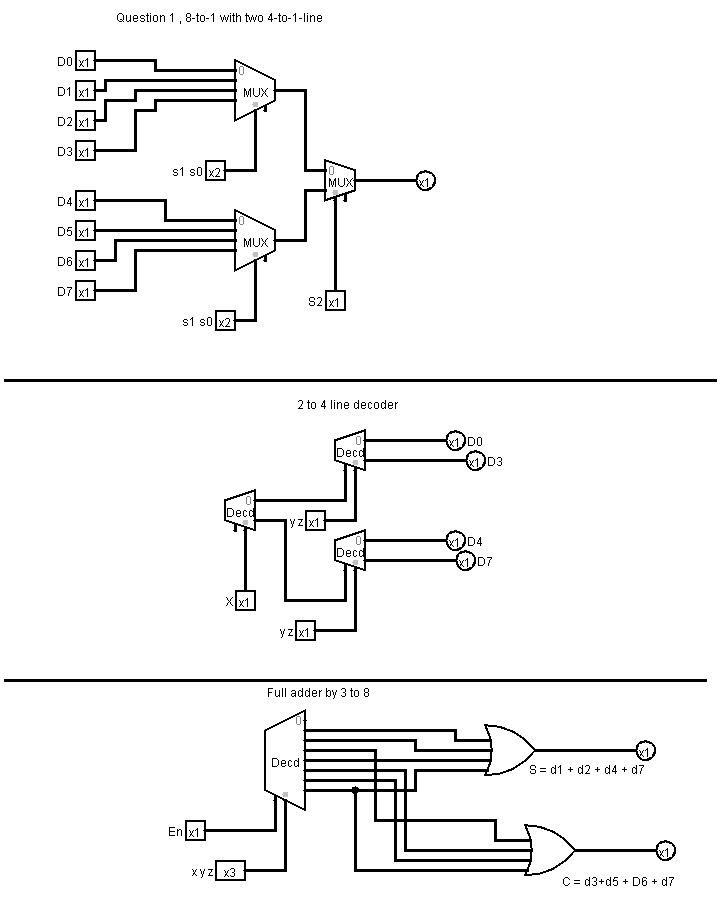
First one is about 8 to 1 multiplexer

The second one is about 2 to 4 decoder

The third is full adder using 3 to 8 decoder

1. **Experiments**

**In the next paper!**



1. **Results**

**8-to-1 multiplexer truth table**

|  |  |  |  |
| --- | --- | --- | --- |
| **S0** | **S1** | **S2** | **F** |
| **0** | **0** | **0** | **D0** |
| **0** | **0** | **1** | **D1** |
| **0** | **1** | **0** | **D2** |
| **0** | **1** | **1** | **D3** |
| **1** | **0** | **0** | **D4** |
| **1** | **0** | **1** | **D5** |
| **1** | **1** | **0** | **D6** |
| **1** | **1** | **1** | **D7** |

**Full adder using 3 to 8 decoder truth table :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **X** | **Y** | **Z** | **S** | **C** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |

**0**

1. **Discussion**

These plexers are combination of basic gates that are useful.